Research Article

Performance Enhancing of Single-Phase Voltage Source Inverter Through Average-Based Pulse Delay Time Compensation

Franklin J[1], *Pongiannan R K*[2,*], *Narayanamoorthi R*[1]

[1]Department of Electrical and Electronic Engineering, SRM Institute of Science and Technology, Kattankulathur, Chennai, India 603203.
[2]Department of Computing Technologies, SRM Institute of Science and Technology, Kattankulathur, Chennai, India 603203.

fj0053@srmist.edu.in, narayanamoorthi.r@gmail.com, pongiank@srmist.edu.in

*Corresponding author: Pongiannan R K; pongiank@srmist.edu.in

DOI: 10.15598/aeee.v22i3.5754

Article history: Received Feb 13, 2024; Revised May 20, 2024; Accepted Jun 26, 2024; Published Sep 30, 2024.

Abstract. *The effectiveness of a Voltage Source Inverter (VSI) operating in a single-phase configuration controlled using Pulse Width Modulation (PWM) depends on multiple factors, particularly a special attention given to the Delay Time (DT) linked to the switching of power devices within the same arm. The ramifications of DT in a single-phase VSI have notable effects on output quality, harmonic content, and transient responsiveness. In this paper, a DT compensator is implemented for a single-phase VSI using the Average Based Pulse Compensation (ABPC) method. This technique adjusts switching instant to counteract the effects of DT and mitigate voltage distortions, reduce harmonic content, and enhance waveform quality. Simulations and validations are performed using MATLAB/Simulink to evaluate compensator performance under different operating conditions. The compensator design is implemented in hardware through the utilization of an FPGA SPARTAN 6 XC6SLX9 controller, tasked with generating a PWM pulse. The quality of ouput voltage and current has been improved by ABP compensation and the THD is reduced by 20%. Additionally, a laboratory testing phase is conducted to assess the performance of the proposed method, involving the validation of a prototype for a single-phase PWM inverter.*

Keywords

Delay time (DT); Single-phase VSI; Average Based Pulse Compensation (ABPC) method; Total harmonic distortion (THD); Field-Programmable Gate Array (FPGA).

1. Introduction

Single-phase VSI play a significant role in various applications such as UPS [1], solar-powered pump [2], and motor drives [3]. The VSI are essential for converting direct current (DC) into alternating current (AC), producing a controlled output voltage waveform with adjustable frequency and magnitude. The efficiency of single-phase VSI lies in the range from 70% to 95%, contingent on factors such as specific design choices, overall system quality, components used, the complexity of switching circuitry, and the operating conditions [4] and [5]. The inverter efficiency is typically high at near the rated output power, and decreases at lower or higher power levels, as indicated by references [6].

The DT is a critical factor that significantly influences voltage distortion as a result of its interaction with non-linear characteristics. Despite their relatively minor magnitude in comparison to switching voltages, voltage dips do not exert the same level of influence

on voltage distortion [7]. Voltage drops in power devices are relatively insignificant when contrasted with the impact of switching voltages. However, the DT predominantly influences the voltage quality and accuracy. The primary strategy for mitigating power losses and enhancing efficiency involves the reduction of switching times. Extended intervals during state transitions create disturbances in the power supply to the load, which subsequently amplifies heat generation and unwarranted energy wastage [8] and [9].

To enhance the efficiency of an inverter, meticulous selection of the switch and switching time becomes imperative, hinging upon the specific requisites of the system and load characteristics. The selection of the switch type in the inverter, be it MOSFETs or IGBTs, significantly influences both the switching time and the overall efficiency of the inverter [10] and [11].

Sinusoidal Pulse Width Modulation (SPWM) and DT are two non-linear factors that exert a significant influence in shaping the harmonic content and total harmonic distortion (THD) of the output parameter. Inverters should meet IEEE and European IEC harmonic design standards, which include limits on total harmonic distortion and harmonic magnitude (IEEE 929, 2000; IEEE 1547, 2003; IEC 61727). The impacts of harmonics are diverse, encompassing concerns related to the quality of electrical energy, stability of the system, and the durability of components [12]. Minimizing the harmonics is grouped into three categories:

- Filter Design involves creating filters to diminish the presence of harmonics [13].
- Selective Compensation is analysing the cause and magnitude of individual harmonics and then applying for compensation. This method requires precise calculations for each harmonic [14].
- The Controller-Based Approach is a closed-loop system and a controller to achieve the desired output voltage and current. It provides flexibility and adaptability, allowing the inverter to respond to changing conditions and requirements in real time [15].

The controller continuously compares the actual output with the desired output and makes adjustments to the switching signals to minimize deviations and achieve the desired performance. To ensure optimal performance of PWM inverters, it is crucial to minimize delays in switching signals. These delays have a negative impact on waveform quality and the overall efficiency of the system [16].

The exploration of DT concepts and its impact on inverter performance includes compensation methodologies like Delay-time compensator (DTC) [17] and [18], Smith Predictor (SP) Compensation [19], Internal Model Control (IMC) [20], and Direct Delay-Time Compensation (DDTC) [21]. These methods, addressing nonlinear behaviour and constant delay time impact of inverter performance parameters such as harmonics, voltage, and current ripples pivot significantly on the DT. Delving into DT Compensation is pivotal in the design of inverter controllers, especially in applications with high speeds or rapid response requirements [22, 23].

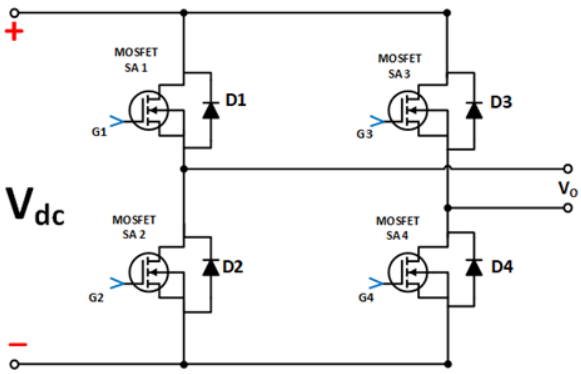


Fig. 1: The common topology of a Single Phase VSI.

The Compensation of delay is designed in MATLAB for a single-phase PWM VSI, and its effect is compensated by using switching intervals directly supplied from the PWM controller circuit [24]. A field-programmable gate array (FPGA) is used to generate SPWM pulses for a single-phase PWM VSI for the compensation of the DT effect [25] and [26]. The DT compensation will be applicable for a motor drive for electric vehicle applications as well as wireless power transfer charging applications [27–29].

Systematically organised, the paper gives a full picture of the study. The effects of DT on single phase inverter performance are thoroughly examined in Section 2. . Later, Section 3. talks about the proposed ABP DTC method and simulation using MATLAB/Simulink and implemented on the FPGA Spartan 6 XC6SLX9 hardware. After this, Section 4. gives a thorough breakdown and review of the output results, focusing on how ABP affect the DT effects and highlighting important findings. Finally, Section 5. summarises the main points of the study and provides the study's results.

2. The Delay Time Demystified: Unraveling Its Impact

The typical single-phase voltage source inverter topology is shown in Figure 1 with the input DC voltgae of

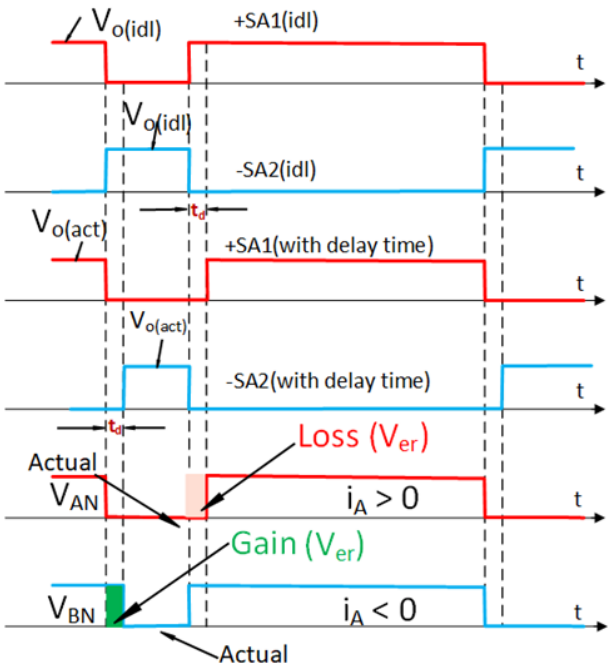
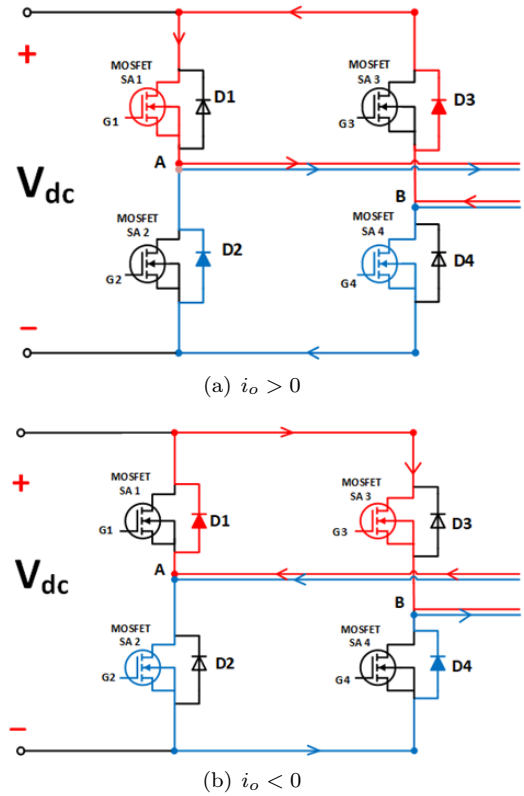


Fig. 2: Influence of the delay time effect on SPWM signals.



(a) $i_o > 0$

(b) $i_o < 0$

Fig. 3: The current path in Single phase inverter with delay time (a) $i_o > 0$, (b) $i_o < 0$.

V_{dc}, and the swtching time of T_s. This topology is the base for our study on the effects of delay time. It gives us a clear way to think about how delay affects the performance of the inverter. The DT in a PWM inverter prevents instantaneous voltage drop to zero during the inactive interval in the lower switch's PWM signal, crucial for short circuit mitigation. Control circuitry presets this delay, influenced by factors like switching frequency and switch characteristics, with insufficient delay risking shoot-through and excessive delay potentially distorting waveforms in single-phase VSI.

In the hypothetical situation where the power switches of the singular arm illustrated in Figure 1 are considered ideal, the possibility arises that both switches (SA1 and SA2) may undergo simultaneous transitions from the OFF to ON states, and vice versa. In practical terms, a fixed delay time (t_d) is present between the gate switches of SA1 and SA2. Figure 2 provides a visual representation of the error occurred in the output voltage due to the influence of DT. This effect becomes apparent during the delay period when switches, as depicted in Figure 3. Influence of the DT effect on the output voltage where two scenarios are considered: Figure 3(a) when $i_o > 0$ and Figure 3(b) when $i_o < 0$.

This delay in switch operation gives rise to non-instantaneous changes in the current flowing through the inductor. Consequently, this current passes through the corresponding antiparallel diodes, leading to a distortion in the voltage. In Figure 2, reference is made to V_{idl} as the ideal output voltage and V_{act} as the actual output voltage. The signals G1–G4 encompass the real drive signals of the switches incorporating the DT.

As demonstrated at point "A" in Figure 3(a), a delay in G1 activation results in both SA1 and SA2 being turned OFF. Subsequently, if the output current i_o is positive, it flows through D2 and SA4 known as i_A. Similarly, the delay in G4 activation leads to the deactivation of SA3 and SA4, as illustrated in point "B". This prompts the current i_o to flow through SA1 and D3 known as i_B or $-i_A$. In both cases mentioned above, the voltage V_{er} deviates from the actual output voltage V_{act} when the output current i_o is greater than zero. The error between $V_{o(idl)}$ and $V_{o(act)}$ is defined as V_{er} known as the voltage drop due to DT and can be expressed as Equation (1),

$$V_{er} = V_{o(idl)} - V_{o(act)}, \tag{1}$$

where V_{er} can be obtained by calculating the average of a single switching period when the i_o direction in arm A represent as $i_o = i_A$:

$$\Delta V_{AN} = +\frac{t_d}{T_s} V_{dc}, \quad \text{if:} i_A > 0, \tag{2a}$$

$$\Delta V_{AN} = -\frac{t_d}{T_s} V_{dc}, \quad \text{if:} i_A < 0. \tag{2b}$$

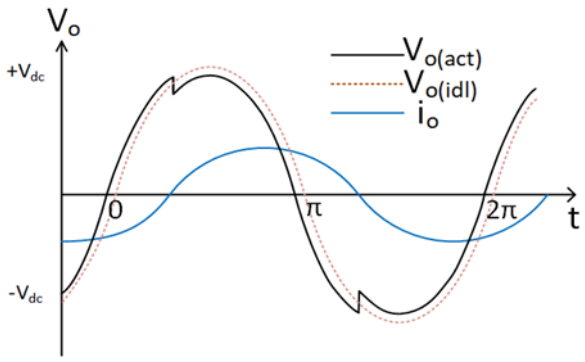


Fig. 4: Influence of DT on the sinusoidal average output voltage.

Equation (2a) and (2b) depict ΔV_{AN} sensitivity to current polarity, directly proportional to DT and inversely related to switching frequency (f_s). Optimal performance, especially with swift switch devices and high frequencies, is attained with a reduced DT.

This analytical paradigm extends seamlessly to arm B in Figure 3(b), noting the inverse correlation ($i_A = -i_B$) between i_A and i_B.

$$\Delta V_{BN} = +\frac{t_d}{T_s} V_{dc}, \quad \text{if:} i_B > 0, \tag{3a}$$

$$\Delta V_{BN} = -\frac{t_d}{T_s} V_{dc}, \quad \text{if:} i_B < 0. \tag{3b}$$

The over all deviation for both leg ΔV_{er}, as expressed by:

$$\Delta V_{er} = \Delta V_{AN} - \Delta V_{BN} = +\frac{2t_d}{T_s} V_{dc}, \quad \text{if:} i_o > 0, \tag{4a}$$

$$\Delta V_{er} = \Delta V_{AN} - \Delta V_{BN} = -\frac{2t_d}{T_s} V_{dc}, \quad \text{if:} i_B < 0. \tag{4b}$$

ΔV_{er} known as the voltage drop due to DT in single arm it also used to as Delay time compensation voltage (V_{dtc}) derived

$$V_{dtc} = \frac{\Delta V_{er}}{2}. \tag{5}$$

The impact of DT is clearly observed in Figure 4 the output voltage and current waveforms indicate a noticeable lag in the load current i_o with respect to the fluctuating $V_{o(act)}$ and $V_{o(dl)}$. This lag becomes particularly prominent during instances of current zero crossing intersections. As a result of this distortion in the output voltage (V_O) at these intersections, it witnesses the emergence of lower-order harmonics, including the 3rd, 5th, and 7th harmonics, in the inverter's output.

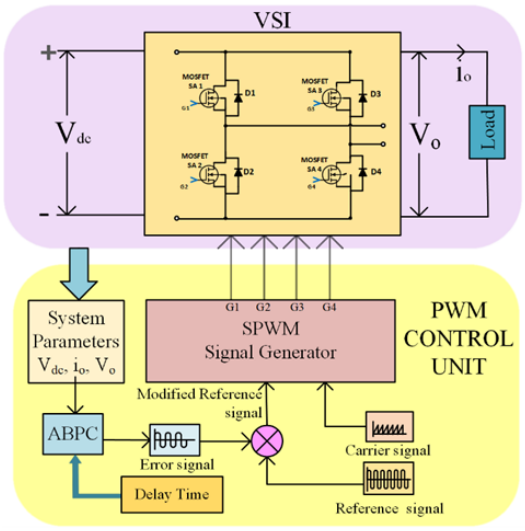


Fig. 5: Working Block diagram of Single Phase Inverter with Average Based Pulse Compensation Method.

3. Implementation of Delay Time Compensation

The PWM inverter employs four methodologies based on design and requisites, including DT insertion and voltage sensing techniques. DT insertion strategically gap between upper and lower switch deactivation-activation. Voltage sensing dynamically adjusts switching timing for device safety. Current sensing is crucial for high-power applications, protecting the inverter and load. Propagation delay compensation and meticulous DT Compensator processes enhance timing precision and synchronization.

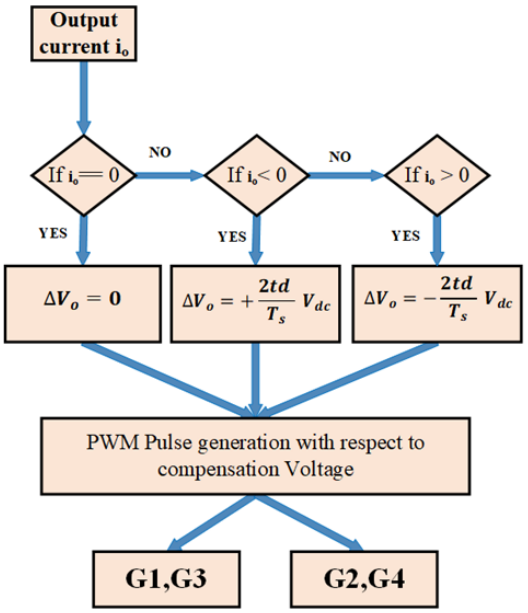


Fig. 6: Flow chart for Average-Based Pulse Compensation method.

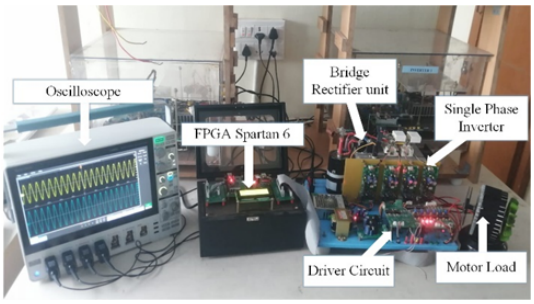


Fig. 7: Experimental setup-FPGA-based ABC Delay Compensator.

3.1. Concepts of Average-Based Pulse Compensation Method

The working block diagram of the single phasae inverter with PWM control unit incorprate with technique of the proposed Average Based Pulse (ABP) compensation method combined with DT, as depicted in Figure 5. Within this method, the reference voltage is dynamically adjusted through addition or subtraction based on the current direction, thereby generating a modified reference waveform. Systematically quantifying the average voltage deviation involves an average-based approach, considering DT and switch voltage drop.

Starting with a PWM generator producing the first sinusoidal pulse width modulation signals required to regulate the inverter's switching transistors, the process proceeds small delays between the switching signals are then introduced using a DT generator to prevent simultaneous conduction, hence avoiding short circuits. This output is filtered to lower harmonics and raise waveform quality. Measuring the actual output, a feedback loop returns this information back to an error detector. The error detector generates an error signal by contrasting the intended and actual outputs. Then, depending on this inaccuracy, a compensation unit changes the SPWM signals to offset DT and guarantee correct and steady AC output.

The flowchart depicts all logical processes within the compensation unit. Recalibrated gate signals are derived from this adjusted reference, as shown in Figure 6 procedural delineation. To account for DT, the PWM signals are changed in response to the detected output current. If $i_o = 0$, there is no need for compensation. If i_o is negative, a positive compensating voltage is used. If i_o is positive, a voltage of opposite polarity is used as compensation.

These adjustments ensure that the SPWM signals precisely reflect the desired output, accounting for any DT and maintaining output quality. The inverter management system significantly reduces DT and maintains a consistent, high-quality AC output by integrating many activities, thereby improving overall performance and dependability.

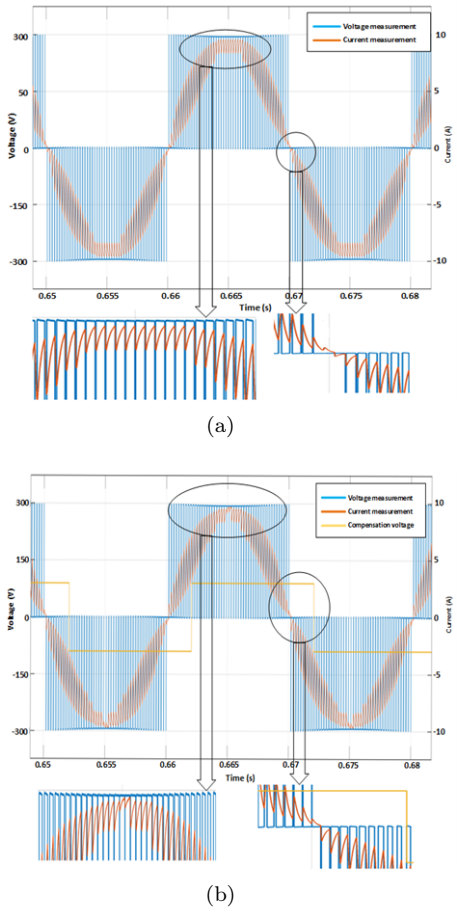


Fig. 8: Simulation Output voltage and current waveform, fo =50Hz, and fs=10 kHz (a) without compensation, (b) with compensation.

3.2. MATLAB/Simulation Model of ABP Compensation

A meticulous MATLAB/Simulink model validates the time domain and Average-Based Pulse (ABP) compensation strategy of a single-phase VSI, employing varied delay times and simulation parameters. The assessment focuses on mitigating the DT effect on output voltage, considering diverse carrier wave ratios and inverter specifications given in Table 1, such as a 300 V rating, switching frequency (f_s) at 10 kHz/5 kHz, with modulation index (m) of 0.9 and for diftrent delay times from 0.5 μs to 2.0 μs. Consider the 20 Ω and 1.5mH set as RL load and it will be lagging approximately 0.65 rad. I_{ref} is 6A with V_{ref} voltage of 10 V peak, with guiding the correct delayed charge for load control. This Analysis involves comparing compensated and uncompensated delay scenarios, moni-

toring effects on load voltage, output current and its Total Harmonic Distortion (THD_{Io}).

Tab. 1: Parameters for Simulation experimental

Parameters	Values
DC voltage (V_{dc})	300 V
switching frequency (f_s)	10 kHz, 5 kHz
Modulation frequency (f_m)	50Hz
Reactor Inductance (L)	1.5mH
Resistance (R)	20 Ω
Delay time (t_d)	0.5 μs, 1.0 μs, 1.5 μs, 2.0 μs

Equation (4a) and (4b) establishes the potential introduction of an error induced by using DT as the compensatory voltage component for the output voltage. Given a specific consideration for DT at 0.5 μs and a switching frequency of 10 kHz, the calculation of the compensation voltage is facilitated given below.

When output current $i_o > 0$

$$\Delta V_{er} = +[(2 * 0.5)/100]V_{dc} = +\frac{V_{dc}}{100}. \tag{6}$$

When output current $i_o < 0$,

$$\Delta V_{er} = -[(2 * 0.5)/100]V_{dc} = -\frac{V_{dc}}{100}. \tag{7}$$

From equation (5), DT compensation voltage V_{dtc} is given by:

$$\begin{aligned} V_{dtc} &= \frac{\Delta V_{er}}{2} \\ V_{dtc} &= +V_{dc}/200, \text{if:} I_o > 0 \\ V_{dtc} &= -V_{dc}/200, \text{if:} I_o < 0 \end{aligned} \tag{8}$$

3.3. FPGA implementation of Average Based Pulse DT Compensation

The hardware experimental setup shown in Figure 7, based on the block diagram ginven in Figure 4, for implementing the ABP DTC in a single-phase inverter involves several key components configured to ensure precise control and accurate measurements. The inverter circuit includes a power stage composed of semiconductor switches, specifically MOSFETs, arranged in an H-bridge configuration to convert the DC input voltage to an AC output. These switches are controlled by a gate driver circuit, such as the IR2110, which provides the necessary isolation and amplification for the control signals. A bridge rectifier is used to convert AC input to DC before feeding it to the inverter stage.

The control board features an FPGA, specifically the Xilinx Spartan-6 XC6SLX9, responsible for implementing the ABP DTC algorithm. This FPGA generates the SPWM signals with precise delay time compensation, ensuring high-speed processing and accurate timing.

For measurement, an oscilloscope, specifically the Keysight DSO-X 2002A, monitors the gate signals and output waveforms, verifying the inverter's operation and the compensation's effectiveness.The load consists of a resistive element, typically a 20 ohm resistor, to simplify the analysis and an inductive component, a 1.2 mH inductor, and the desinging parameters values ginven in Table 2.

Tab. 2: The parameters used for proposed system in FPGA hardware experiment

Parameters	Values
DC voltage (V_{dc})	325 V
switching frequency (f_s)	10 kHz, 5 kHz
Modulation frequency (f_m)	50Hz
Reactor Inductance (L)	1.5mH
Resistance (RL)	20 Ω
Delay time (t_d)	0.5 μs, 1.0 μs, 1.5 μs, 2.0 μs

The procedure starts with initializing the connections from the DC power supply to the inverter and from the inverter output to the resistive and inductive loads. The FPGA is then programmed with the ABP DTC algorithm using appropriate development tools.

Upon powering the DC supply, the inverter operation begins, and the FPGA generates the PWM signals with ABP DTC. Data from the oscilloscope is recorded for different delay times and switching frequencies. The results are analyzed to compare the performance improvements brought by ABP DTC, focusing on harmonic reduction and output quality enhancement. The detailed results analysis given in the next section.

4. Results and Discussion

The ABP compensation method has been designed and simulated in MATLAB 2017a and the model is implemented in an FPGA SPARTAN 6 XC6SLX9. The results are discussed in this session.

4.1. Simulation Results and Discussion

The simulation results are presented in Table 3. It is evident that as the delay time increases, there is a corresponding decrease in output voltage and current, accompanied by an increase in Total Harmonic Distortion (THD). The implementation of ABP DT compensation simultaneously reduces THD while increasing output voltage and current. A MATLAB model of a single-phase inverter was simulated at switching frequencies of 5 kHz and 10 kHz. The fundamental voltage and

current, along with the Total Harmonic Distortion of Current (THD_{Io}), and the percentages of third harmonic voltage and current, are determined for every possible combination of DT (0.5 μs, 1.0 μs, 1.5 μs, and 2.0 μs), both with and without ABP compensation.

Tab. 3: Simulation results for the inverter with 20 Ω and 1.5mh RL load for different DT 0.5 μs, 1.0 μs 1.5 μs, and 2.0 μs

DT	Switching frequency (fs)	ABP compensation	Fundamental			3rd harmonic	
			V (%)	I (A)	THD_{Io} (%)	V (%)	I (%)
0.5 μs	10 kHz	NO	97.8	5.5	5.2	0.72	0.56
		YES	99.5	6.2	4.2	0.16	0.13
	5 kHz	NO	78.2	4.4	5.7	0.58	0.45
		YES	79.6	4.9	4.6	0.13	0.10
1.0 μs	10 kHz	NO	96.3	4.7	5.3	0.88	0.76
		YES	98.5	5.9	4.4	0.55	0.33
	5 kHz	NO	77.0	3.7	5.9	0.70	0.61
		YES	78.8	4.7	4.8	0.44	0.26
1.5 μs	10 kHz	NO	95.4	5.5	5.4	1.42	1.26
		YES	98.7	5.8	4.7	0.95	0.92
	5 kHz	NO	76.3	4.4	5.9	1.14	1.01
		YES	78.9	4.6	5.2	0.76	0.74
2.0 μs	10 kHz	NO	94.4	4.7	5.5	1.88	1.56
		YES	98.2	5.8	4.6	1.15	1.05
	5 kHz	NO	75.5	3.7	6.1	1.50	1.25
		YES	78.5	4.6	5.0	0.92	0.84

The output voltage and current waveforms10kHz swithcing freequmcy with Fundamental frequency of 50Hz shown in Figure 8. Figure 8(a) is the without DT compensation with two insights of peak and zero crossing votage and current waveforms in that the presence of peak distortion leads to reduced power delivery efficiency and increased harmonic distortions.as same as Figure 8(b) denoted the with DT compensation alomg with two insights of peak and zero crossing waveforms exhibits smooth, regular characteristics with minimal distortion, indicating effective delay-time management and optimal switching performance. This results in efficient power delivery with minimized harmonic content. Comparing compensated and uncompensated output voltage and current, peaks exhibit non-sinusoidal currents in Figure 8(a) and Figure 8(b). Voltage drop in the zero-crossing zone induces current lag, mitigated in compensated waveforms.

Without ABP compensation, the fundamental voltage drops as the DT increases. For instance, at 10 kHz and 0.5 μs DT, the fundamental voltage is 97.8%, but at 2.0 μs, it drops to 94.40%. With ABP compensation, this drop is mitigated, maintaining values close to ideal (98.5% - 99.5%).At 5 kHz and 0.5 μs DT, the fundamental voltage is 78.2%, dropping to 75.5% at 2.0 μs. With ABP compensation, the values are improved, ranging from 79.6% to 78.5%.Without ABP compensation, increasing DT reduces the fundamental voltage and increases THD_{Io} and 3rd harmonics significantly.

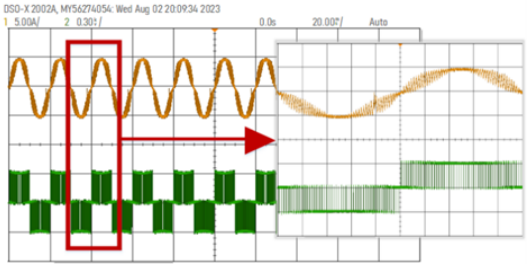


Fig. 9: Output voltage (Green trace) and current (Orange trace) waveforms for 1.0 μs delay time with compensation.

Fig. 10: SPWM gate pulses (orange, green traces) for upper and lower in single leg with DT 1.0 μs.

Without compensation, the 3rd harmonic increases with DT. With ABP compensation, these values drop significantly, indicating better harmonic suppression.For instance, at 10 kHz and 2.0 μs DT, the 3rd harmonic voltage is 1.88%, and current is 1.56%. For instance, at 10 kHz and 2.0 μs DT, THD_{Io} is 5.5% without compensation and reduces to 4.6% with ABP compensation. This shows that ABP compensation significantly reduces THD_{Io}, improving output quality.

With ABP compensation, the fundamental voltage and current are closer to ideal values, with notable improvements in reducing THD_{Io} and harmonic distortions. The ABP compensation effectively mitigates the adverse effects of DT, maintaining higher performance and lower distortion levels in inverter output, particularly at higher switching frequencies (10 kHz). Notably, the 0.5 μs DT in switching poses a higher risk of short circuits compared to the compensated operation at 2.0 μs.

4.2. Experimental Results and Discussions

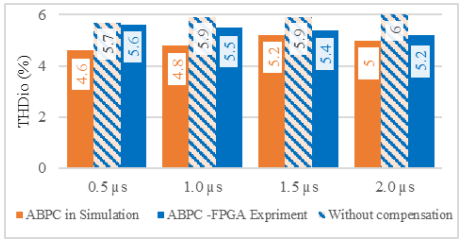
The provided Table 4 showcases the impact of delay time (DT) and switching frequency (f_s) on the performance metrics of a single-phase inverter, particularly focusing on the fundamental voltage and current, as well as the 3rd harmonic voltage and current percentages. The data is presented for various delay time values (0.5 μs, 1.0 μs, 1.5 μs, and 2.0 μs) and two differ-

ent switching frequencies (5 kHz and 10 kHz), with and without ABP compensation implemented in an FPGA Spartan 6 XC6SLX9 board.

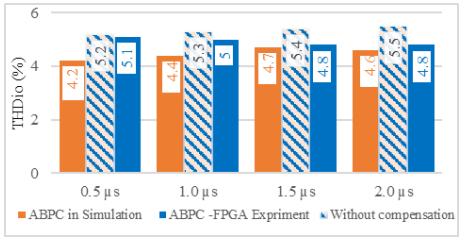
Tab. 4: Experimental results of compensated output of the inverter with 20 Ω and 1.5mh RL load for DT 0.5 μs, 1.0 μs 1.5 μs, and 2.0 μs.

DT	Switching frequency (fs)	Fundamental			3rd harmonic	
		V (%)	I (A)	TDH_{Io} (%)	V (%)	I (%)
0.5	10 kHz	98.89	5.91	5.17	0.98	0.66
μs	5 kHz	79.11	4.73	5.69	0.78	0.53
1.0	10 kHz	97.88	5.82	5.02	0.55	0.33
μs	5 kHz	78.30	4.66	5.52	0.44	0.26
1.5	10 kHz	97.20	4.92	4.94	1.88	1.56
μs	5 kHz	77.76	3.94	5.44	1.50	1.25
2.0	10 kHz	97.10	4.86	4.81	1.15	1.05
μs	5 kHz	76.88	3.89	5.29	0.92	0.84

With ABP compensation implemented, at a delay time of 0.5 μs and a switching frequency of 10 kHz, the fundamental voltage percentage is 98.89%, the fundamental current is 5.91 A, and the Total Harmonic Distortion of Current (THD_{Io}) is 5.17%. Similarly, at a delay time of 1.0 μs and a switching frequency of 5 kHz, the fundamental voltage percentage decreases to 78.30%, with a fundamental current of 4.66 A and THD_{Io} of 5.52%. As delay time increases to 1.5 μs and 2.0 μs, there's a noticeable drop in both fundamental voltage percentage and current, accompanied by an increase in THD_{Io}.



(a) 5 kHz



(b) 10 kHz.

Fig. 11: Comparison Graph of THDio Without compensation, with ABP compensation in simulation and FPGA experimental values (a) 5 kHz (b) 10 kHz.

Comparing the results with and without ABP compensation, it's evident that ABP compensation consistently improves performance metrics. For instance, at a delay time of 1.0 μs and a switching frequency of

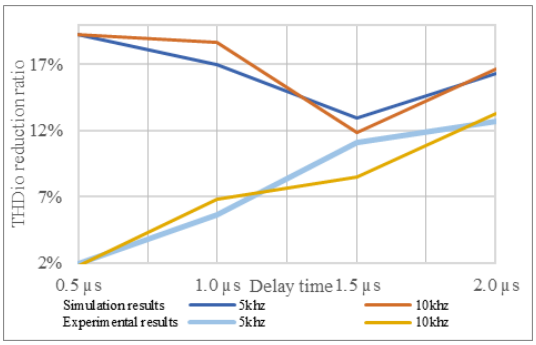


Fig. 12: THD_{Io} reduction ratio from Without compensation results to with ABP compensation in Simulation and FPGA experimental values.

10 kHz, without compensation, the fundamental voltage percentage is 97.88% and THDIo is 5.02%, whereas with compensation, the fundamental voltage percentage slightly increases to 98.89%, and THDIo decreases to 0.55%. This indicates that ABP compensation effectively enhances output voltage and current while reducing harmonic distortion, thereby optimizing the performance of the single-phase inverter.

The compensation effect of the ABP method is illustrated in Figure 9. Notably in insights, the current waveform continues to display some distortion in the zero-crossing region. The generated SPWM gate signals along with a DT of 1.0 μs and DT detection shown in Figure 10. This stems from the ABPC method's dependence on current zero-crossing detection, potentially leading to control delays and misinterpretation of current polarity. Additionally, the suppression of low-frequency harmonics is not entirely effective.

Figure 10 depicts SPWM pulses generated by the FPGA SPARTAN 6 XC6SLX9 in order to compensate for the delay time effect using the ABP method with a delay time of $t_d = 1.0\mu s$ inserted between the upper and lower legs.

Figure 11(a) is comparison graph view of the THD of output current with and without compensation at 5 kHz switching frequency. Without compensation, delay time leads to increased THD_{Io} and reduce the performance, THD_{Io} increases from 5.7% to 6% for the delay times 0.5 μs to 2.0 μs. The implementation of ABP DTC in simulations considerably minimizes THD_{Io} and harmonic distortions across all delay times. THD_{Io} decreases from 5.7 % to 4.6 at 0.5 μs. Implementing ABP DTC in simulation reduces the THD significantly for other delay time values, highlighting its effectiveness. The FPGA implementation of ABP DTC yields comparable or somewhat better results than without compensation, THD_{Io} reduced from 6.0% to 5.2% at 2.0 μs with correction The FPGA implementation achieves comparable or slightly better

THD_{Io} reduction for all delay time values, demonstrating its practical applicability.

Figure 11(b) is comparison graph view of the THD_{Io} of output current with and without compensation at 10 kHz switching frequency. Without compensation, delay time leads to increased THD_{Io} and reduce the performance. The THD_{Io} increases from 5.2% at 0.5 μs to 5.5% at 2.0 μs. When comparing with Simulation results ABP DTC shows effectively reduced the THD_{Io} from 5.7% to 4.6% for 0.5 μs delay times. When comparing with FPGA-implemented experiment results the THD_{Io} similarly reduced from 5.5% to 4.8% at 2.0 μs. Showcasing its robustness and reliability in real-world applications. The THD_{Io} without compensation also increases with delay time, reflecting a decline in output quality.

Figure 12 is graphical representation of the THD_{Io} reduced ratio between without compensation vs simulation results as well hardware results of output current for both 5 kHz and 10 kHz switching frequency. The simulation shows for both 5 kHz and 10 kHz frequencies the ABP compensation reduces the THD_{Io} from 12% to 20 % over the delay times 0.5 μs to 2.0 μs. But practically the ABP compensation reduces the THD_{Io} from 2% to 14 % over the delay times 0.5 μs to 2.0 μs. It's made confirmed the increasing the delay time make THD_{Io} increases also affect the overall performance of the inverter.

These comparisons illustrate that both simulation and FPGA implementations of ABP DTC significantly improve inverter performance by reducing THD_{Io} up to 20% and harmonic distortions, with the FPGA implementation offering a practical, high-performing solution. The study analyzed THDio percentages for different switching frequencies and delay times. The Simulation ABP DTC method achieved the lowest THDio across all delay times, demonstrating the most effective reduction in harmonic distortion compared to uncompensated. The results suggest that ABP DTC is the most effective method for reducing harmonic distortion even the long delay time choose for higher and lower switching frequencies.

5. Conclusion

In this paper, the DT effect on single-phase VSI is analyzed using a MATLAB/Simulink model, and also the DT compensators are implemented using an FPGA solution, and the output parameters are discussed in detail. DT creates harmonics in output voltage and current leading to reduce the efficiency of the PWM VSI. The Average-Based Pulse compensation method is implemented to compensate for the DT effects. The implementation of ABP DTC, both in simulation and FPGA, significantly improves the performance of single-phase inverters by reducing THDIo up to 20% and harmonic distortions, even as delay time increases. The FPGA-based solution offers a robust and reliable method for real-world applications, maintaining high output quality under varying conditions. These findings underscore the value of ABP DTC in enhancing inverter efficiency and effectiveness, making it a viable option for practical deployment in power electronics systems.

References

[1] DENG, H., R. ORUGANTI and D. SRINIVASAN. PWM methods to handle time delay in digital control of a UPS inverter. *IEEE Power Electron. Letters*. 2005, vol. 3, no. 1, pp. 1-6. DOI: 10.1109/LPEL.2004.842402.

[2] AZARUDEEN and D. MARY. Performance analysis of conventional and digital PWM control scheme for speed control of BLDC motor drives. In: *Proc. Int. Conf. on Advances in Electr. Tech. for Green Energy*. India : IEEE, 2017, pp. 69-75, DOI: 10.1109/ICAETGT.2017.8341460.

[3] PONGIANNAN, R. K., et al. Non-isolated coupled converter tied voltage source inverter drive. *Int. J. of Power Electron. and Dri. Sys.* 2019, vol. 10, no. 2 pp. 645-652. DOI: 10.11591/ijpeds.v10.i2.pp645-652.

[4] PONGIANNAN, R. K., et al. A simple switching on-time calculation revision in multilevel inverter-space vector modulation to achieving extended voltage boundary operation. Int. J. of Power Electron. And Dri. Sys. 2019, vol. 10 no. 2. DOI: 10.11591/ijpeds.v10.i2.653-661.

[5] YANG, Y., K. ZHOU, and F. BLAABJERG. Analysis of dead-time harmonics in single-phase transformerless full-bridge PV inverters. In: *Proc. IEEE Appl. Power Electronics Conference and Exposition 2018*. San Antonio, TX, USA: IEEE, 2018, pp. 1310-1315, DOI: 10.1109/APEC.2018.8341186.

[6] LEWICKI. Dead-Time Effect Compensation Based on Additional Phase Current Measurements. *IEEE Trans. on Ind. Electron.* 2015, vol. 62, no. 7, pp. 4078-4085. DOI: 10.1109/TIE.2015.2389756.

[7] WEERAKOON, D. B. R., B. L. L. SANDARUWAN, R. T. T. De SILVA, S. G. ABEYRATNE and D. B. RATHNAYAKE. A novel dead-time compensation scheme for PWM

VSI drives. In: *Proc. IEEE International Conference on Information and Automation for Sustainability.* , Galle, Sri Lanka: IEEE, 2016, pp. 1-6, DOI: 10.1109/ICIAFS.2016.7946570.

[8] WANG, Y., W. XIE, X. WANG and D. GERLING. A Precise Voltage Distortion Compensation Strategy for Voltage Source Inverters. *IEEE Transactions on Industrial Electronics.* 2018, vol. 65, no. 1, pp. 59-66. DOI: 10.1109/TIE.2017.2716866.

[9] PONGIANNAN, R. K., S. PARAMASIVAM, and N. YADAIAH. FPGA realisation of an area efficient SVPWM modulator for three phase induction motor drive. *International Journal of Power Electronics*, 2010, vol. 2, no.2, pp: 176-199. DOI: 10.1504/IJPELEC.2010.031193.

[10] YANG, Y., K. ZHOU, H. WANG, and F. BLAABJERG. Analysis and Mitigation of Dead-Time Harmonics in the Single-Phase Full-Bridge PWM Converter with Repetitive Controllers. *IEEE Transactions on Industry Applications.* 2018, vol. 54, no. 5, pp. 5343-5354. DOI: 10.1109/TIA.2018.2825941.

[11] FRANKLIN J, R. PRAVIN A and PONGIANNAN R K. The Performance Analysis of Single Phase PWM Inverter with Various Delay Times. In: *Proc. International Conference on Circuit Power and Computing Technologies.* India: IEEE, 2023, pp. 1414-1419. DOI: 10.1109/ICCPCT58313.2023.10245085.

[12] CHENG, J., D. CHEN, G. CHEN. Modelling and Compensation for Dead-Time Effect. in High Power IGBT/IGCT Converters with SHE-PWM Modulation. *Energies.* 2020, vol. 13, pp. 4348. DOI: 10.3390/en13174348

[13] CHIERCHIE, F., E. E. PAOLINI and L. STEFANAZZI. Dead-Time Distortion Shaping. *IEEE Transactions on Power Electronics.* 2019, vol. 34, no. 1, pp. 53-63. DOI: 10.1109/TPEL.2018.2825218.

[14] PONGIANNAN, R. K., P. SELVABHARATHI, and N. YADAIAH. FPGA based three-phase sinusoidal PWM VVVF controller. In: *Proc. IEEE International Conference on Electrical Energy Systems.* Chennai, India: IEEE, 2011, pp. 34-39. DOI: 10.1109/ICEES.2011.5725298.

[15] JIN, T., X. SHEN, T. SU and R. C. C. FLESCH. Model Predictive Voltage Control Based on Finite Control Set with Computation Time Delay Compensation for PV Systems. *IEEE Transactions on Energy Conversion.* 2019, vol. 34, no. 1, pp. 330-338. DOI: 10.1109/TEC.2018.2876619.

[16] CHUN, Z., M. QISHUANG, C. TONGKAI and Z. POMING. Model-predictive current control of DC/AC inverters with time delay compensation. In: *Proc. IEEE International Conference on Aircraft Utility Systems.* China: IEEE, 2016, pp. 398-402. DOI: 10.1109/AUS.2016.7748082.

[17] SAWACHAN, H., P. LIUTANAKUL and N. WIWATCHARAGOSES. A simple dead-time compensation technique for single-phase full-bridge PWM rectifier. In: Proc. International Electrical Engineering Congress. Pattaya, Thailand: IEEE, 2017, pp. 1-4. DOI: 10.1109/IEECON.2017.8075757.

[18] PONGIANNAN, R. K., S. PARAMASIVAM, and N. YADAIAH. Dynamically reconfigurable PWM controller for three-phase voltage-source inverters. *IEEE Transactions on Power Electronics.* 2010, vol. 26, no. 6, pp:1790-1799. DOI: 10.1109/TPEL.2010.2066577.

[19] LUO, Y., W. XUE, W. HE, K. NIE, Y. MAO and J. M. GUERRERO. Delay-Compound-Compensation Control for Photoelectric Tracking System Based on Improved Smith Predictor Scheme. *IEEE Photonics Journal.* 2022, vol. 14, no. 3, pp. 1-8, DOI: 10.1109/JPHOT.2022.3164202.

[20] ZHANG, X., and C. ZHANG. Model Predictive Control for Open Winding PMSM Considering Dead-Zone Effect. *IEEE Journal of Emerging and Selected Topics in Power Electronics.* 2023, vol. 11, no. 1, pp. 874-885. DOI: 10.1109/JESTPE.2022.3207186.

[21] KAVIMANDAN, U. D., V. P. GALIGEKERE, O. ONAR, B. OZPINECI and S. M. MAHAJAN. Comparison of Dead-Time Effects in a WPT System Inverter for Different Fixed-Frequency Modulation Techniques. In: *Proc. IEEE Transportation Electrification Conference & Expo.* Chicago, IL, USA: IEEE, 2020, pp. 277-283. DOI: 10.1109/ITEC48692.2020.9161646.

[22] HERRAN, M. A., J. R. FISCHER, S. A. GONZALEZ, M. G. JUDEWICZ and D. O. CARRICA. Adaptive Dead-Time Compensation for Grid-Connected PWM Inverters of Single-Stage PV Systems. *IEEE Trans. on Power Electron.* 2013, vol. 28, no. 6, pp. 2816-2825. DOI: 10.1109/TPEL.2012.2227811.

[23] RATHNAYAKE D. B., S. M. H. K. SAMARASINGHE, C. I. MEDAGEDARA and S. G. ABEYRATNE. An enhanced pulse-based dead-time compensation technique for PWM-VSI drives. In: *Proc. International Conference on Industrial and Information Systems.* In-

dia: IEEE, 2014, pp. 1-5. DOI: 10.1109/ICIINFS.2014.7036532.

[24] KAVIMANDAN, U. D., V. P. GALIGEKERE, B. OZPINECI, O. ONAR and S. M. MAHAJAN. The Impact of Inverter Dead-Time in Single-Phase Wireless Power Transfer Systems. *IEEE Transactions on Power Electronics*. 2022, vol. 37, no. 1, pp. 1074-1089. DOI: 10.1109/TPEL.2021.3092400.

[25] PONGIANNAN, R. K., and N. YADAIAH. FPGA based Space Vector PWM Control IC for Three Phase Induction Motor Drive. In: *Proc. IEEE International Conference on Industrial Technology*. India: IEEE, 2006, pp. 2061-2066. DOI: 10.1109/ICIT.2006.372493.

[26] PONGIANNAN, R. K., et al. A simple multilevel space vector modulation technique and MATLAB system generator-built FPGA implementation for three-level neutral-point clamped inverter. *Energies*. 2019, vol. 12, no. 22, pp: 4332. DOI: 10.3390/en12224332.

[27] SUBUDHI, P. S., S. PADMANABAN, F. BLAABJERG, and D. P. KOTHARI. Design and Implementation of a PV fed Grid Integrated Wireless Electric Vehicle Battery Charger Present in a Residential Environment. *IEEE Journal of Emerging and Selected Topics in Industrial Electronics*. 2022, vol. 4, no. 1, pp. 78 - 86. DOI: 10.1109/JESTIE.2022.3195087.

[28] SHANMUGAM, Y., et al. A systematic review of dynamic wireless charging system for electric transportation. *IEEE Access*. 2022, vol. 10, pp. 133617 - 133642. DOI: 10.1109/ACCESS.2022.3227217.

[29] VENKATESAN, N. R., et al. A Review of Compensation Topologies and Control Techniques of Bidirectional Wireless Power Transfer Systems for Electric Vehicle Applications. *Energies*. 2022, Vol. 15, no. 20, pp: 7816. DOI: 10.3390/en15207816.